In the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-27 Canceled.

28. (Previously Presented) A semiconductor memory device comprising:

a first power line for receiving a power voltage;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

a selection circuit for outputting selection signals for selecting for testing the rows in one of the repair units in response to a row address;

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, in a test operation mode such that power is turned off from the rows of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing,

wherein the switch circuit comprises switches, each of the switches connected to a corresponding second power line, wherein each of the switches comprises:

a NOR gate for receiving the control signal and a corresponding selection signal, and

a PMOS transistor for connecting the first power line with a corresponding second power line in response to an output signal of the NOR gate.

29. (Original) The semiconductor memory device of claim 28, further comprising first and second pads for respectively receiving the power voltage.

30. (Original) The semiconductor memory device of claim 29, wherein the first power line is directly connected to the second pad and is connected to the first pad through a switch transistor.

31. (Previously Presented) A semiconductor memory device comprising:

a first power line for receiving a power voltage;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

a selection circuit for outputting selection signals for selecting for testing the rows in one of the repair units in response to a row address;

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, in a test operation mode such that power is turned off from the rows of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing; and

first and second pads for respectively receiving the power voltage,

wherein the first power line is directly connected to the second pad and is connected to the first pad though a switch transistor, and

wherein the switch transistor is controlled by a control signal that is based on whether the semiconductor memory device is in the test operation mode.

32. (Original) The semiconductor memory device of claim 28, wherein the first power line is connected to a pad for receiving the power voltage.

33. (Canceled)

34. (Previously Presented) The semiconductor memory device of claim 28, wherein each of the switches further comprises a fuse connected between the PMOS transistor and a corresponding second power line.

35. (Original) The semiconductor memory device of claim 34, wherein in the test operation mode, whether the memory cells of the selected rows comprise the memory cell having standby current failure is judged depending on variation of the power voltage.

36. (Original) The semiconductor memory device of claim 35, wherein each of the fuses is cut when the memory cells of corresponding rows comprise the memory cell having the standby current failure.

37. (Original) The semiconductor memory device of claim 28, further comprising a precharge circuit for precharging the columns.

38. (Original) The semiconductor memory device of claim 37, wherein the precharge circuit is inactivated during the test operation mode.

39. (Previously Presented) A semiconductor memory device comprising:

a first power line for receiving a power voltage;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

a selection circuit for outputting selection signals for selecting for testing the columns in one of the repair units in response to a column address;

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals and disconnecting the remaining second power lines from the first power line, in a test operation mode such that power is turned off from the rows of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing,

wherein the switch circuit comprises switches, each of the switches connected to a corresponding second power line, wherein each of the switches comprises:

a NOR gate for receiving the control signal and a corresponding selection signal, and

a PMOS transistor for connecting the first power line with a corresponding second power line in response to an output signal of the NOR gate.

40. (Original) The semiconductor memory device of claim 39, further comprising first and second pads for respectively receiving the power voltage.

41. (Original) The semiconductor memory device of claim 40, wherein the first power line is directly connected to the second pad and is connected to the first pad through a switch transistor.

42. (Previously Presented) A semiconductor memory device comprising:

a first power line for receiving a power voltage;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

a selection circuit for outputting selection signals for selecting for testing the rows in one of the repair units in response to a row address;

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, in a test operation mode such that power is turned off from the rows of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing; and

first and second pads for respectively receiving the power voltage,

wherein the first power line is directly connected to the second pad and is connected to the first pad though a switch transistor, and

wherein the switch transistor is controlled by a control signal that is based on whether the semiconductor memory device is in the test operation mode.

43. (Original) The semiconductor memory device of claim 39, wherein the first power line is connected to a pad for receiving the power voltage.

44. (Canceled)

45. (Previously Presented) The semiconductor memory device of claim 39, wherein each of the switches further comprises a fuse connected between the PMOS transistor and a corresponding second power line.

46. (Original) The semiconductor memory device of claim 45, wherein in the test operation mode, whether the memory cells of the selected columns comprise the memory cell having standby current failure is judged depending on variation of the power voltage.

47. (Original) The semiconductor memory device of claim 46, wherein each of the fuses is cut when the memory cells of corresponding columns comprise the memory cell having the standby current failure.

48. (Original) The semiconductor memory device of claim 39, further comprising a precharge circuit for precharging the columns.

49. (Original) The semiconductor memory device of claim 48, wherein the precharge circuit is inactivated during the test operation mode.

50. (Canceled)

51. (Previously Presented) A semiconductor memory device comprising:

a first power line for receiving a power voltage;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit;

a selection circuit for outputting selection signals for selecting for testing one of the repair units; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, in a test operation mode such that power is turned off from the repair units of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing; and

first and second pads for respectively receiving the power voltage,

wherein the first power line is directly connected to the second pad and is connected to the first pad though a switch transistor, and

wherein the switch transistor is controlled by a control signal that is based on whether the semiconductor memory device is in the test operation mode.

Claims 52-54 Canceled.

55. (Previously Presented) The semiconductor memory device of claim 51, wherein the switch circuit comprises switches, each of the switches connected to a corresponding second power line, wherein each of the switches comprises:

a NOR gate for receiving the control signal and a corresponding selection signal; and

a PMOS transistor for connecting the first power line with a corresponding second power line in response to an output signal of the NOR gate.

56. (Original) The semiconductor memory device of claim 55, wherein each of the switches further comprises a fuse connected between the PMOS transistor and a corresponding second power line.

57. (Original) The semiconductor memory device of claim 51, wherein in the test operation mode, whether the memory cells of the selected repair unit comprise the memory cell having standby current failure is judged depending on variation of the power voltage.

58. (Original) The semiconductor memory device of claim 56, wherein each of the fuses is cut when the memory cells of corresponding columns comprise the memory cell having the standby current failure.